CLAIMS

What is claimed is:

1. A semiconductor memory device including a plurality of memory cells, the semiconductor memory device comprising:

an input buffer that respectively writes signature fuse data related to signature fuses to the memory cells when the semiconductor memory device enters a test mode; and

an output buffer that reads the signature fuse data from the memory cells during a normal read operation of the semiconductor memory device,

wherein the signature fuse data comprises binary data that is determined based on whether the respective signature fuse is cut.

2. The semiconductor memory device of claim 1, wherein the input buffer writes one of the signature fuse data and input data, which is generated during a normal write operation of the semiconductor memory device, to the respective memory cells in response to a command signal which is synchronized with a clock signal and a combination of address signals.

3. The semiconductor memory device of claim 2, wherein the input data is initialization data at a low level "0" that is written to the memory cells prior to writing of the signature fuse data to the respective memory cells.

4. The semiconductor memory device of claim 3, wherein the semiconductor memory device further comprises:

a fuse box selection circuit that decodes the command signal which is synchronized with the clock signal and the combination of the address signals and generates a plurality of selection signals; and

a plurality of fuse boxes including the signature fuses that output the signature fuse data in response to the selection signals, respectively.

5. The semiconductor memory device of claim 4, wherein the address signal for selecting the respective fuse boxes is the same as the address signal for selecting the respective memory cells to which the signature fuse data is written.

6. The semiconductor memory device of claim 5, wherein the command signal that is in phase with the clock signal and a combination of the address signals enable the semiconductor memory device to enter or exit a signature fuse read mode that is the test mode.

7. The semiconductor memory device of claim 6, wherein the address signal is one of an externally generated address signal and an internal address signal generated in an internal address generator of the semiconductor memory device.

8. A method of reading data regarding signature fuses in a semiconductor memory device, the method comprising:

(a) entering a signature fuse read mode in response to a command signal that is in phase with the clock signal and a combination of address signals;

(b) outputting signature free data related to signature fuses included in fuse boxes selected in response to the address signal;

(c) writing the output signature fuse data to memory cells selected in response to the address signal that is the same as the address signal used in (b);

(d) exiting the signature fuse read mode in response to a command signal that is in phase with a clock signal and the combination of address signals; and

(e) reading the signature fuse data from the memory cells through a normal read operation of the semiconductor memory device.

9. The method of claim 8, wherein (a) comprises initializing the memory cells by writing data at a low level "0" to the memory cells through a normal write operation.

10. The method of claim 9, wherein (c) further comprises determining whether data related to a signature fuse to be written to a corresponding memory cell concerns a last signature fuse, and continuing to write data regarding the signature fuses to the corresponding memory cells until the signature fuse data of the last signature fuse is written to the memory cells.

11. A method of reading data regarding signature fuses in a semiconductor memory device, the method comprising:

(a) entering a signature fuse read mode in response to a command signal that is in phase with a clock signal and a combination of internal address signals;

(b) outputting signature fuse data related to signature fuses that are included in respective fuse boxes selected in response to the internal address signal;

(c) writing the output signature fuse data to memory cells selected in response to the internal address signal that is the same as the internal address signal used in (b);

(d) exiting the signature fuse read mode in response to a command signal that is in phase with a clock signal and a combination of address signals; and

(e) reading the written signature fuse data from the memory cells through a normal read operation of the semiconductor memory device.

12. The method of claim 10, wherein (a) further comprises initializing the memory cells by writing data at a low level "0" to the memory cells through a normal write operation of the semiconductor memory device.